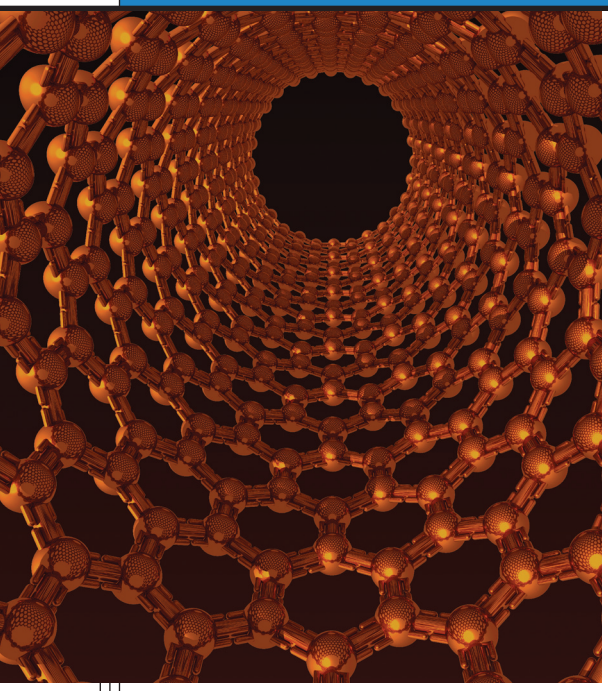

# Transitioning from Microelectronics to Nanoelectronics

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**By breaking down abstractions and facing challenges in an integrated fashion from the devices up, designers could develop novel systems that ultimately go beyond von Neumann processing on silicon.**

For more than 50 years, visionaries have heralded the prospect of a nanoelectronic computer built from the atoms or molecules up. For nearly as long, many have predicted the demise of the silicon microelectronic technology underlying conventional computing as we know it.

However long it takes silicon to breathe its last gasp, the time is coming when the computing industry must look elsewhere for the means to sustain the rapid increase in capability that has enabled the development of a wide range of new applications, as well as large, profitable markets for memories and processors.

## KEY CHALLENGES

Anticipating this new era, a growing research community has coalesced around the two key challenges of computing without silicon microelectronics:

- inventing a scalable device and fabrication technology to replace the transistor, and
- designing architectures for systems that can perform information processing using such devices.

For many computer architects, the first challenge takes priority. After all, we are used to operating under the protection of well-designed abstractions that permit our architectures to accommodate anything from ideal switches to the least palatable of devices that might be foisted upon us. However, the nanodevices that prevail over silicon seem destined to break even the sturdiest of abstractions. The relationships between computation and communication shift as we approach the nanometer scale, such that novel nanodevices impose new rules about the partitioning and allocation of "code" and "data," for example. This can be a blessing in disguise: although it requires system designers to look beyond stored-program architectures with which they are comfortable, it also liberates them to work with new hardware primitives. In fact, postsilicon nanodevices might not even compute in a binary fashion.

Thus, several standout nanocomputer architects have adopted a more transcendent approach that also addresses the second key challenge. They have realized that by breaking down abstractions and facing challenges in an integrated fashion from the devices up, novel systems might be developed that ultimately go beyond von Neumann processing on silicon. Moreover, some have taken steps to demonstrate how this could be accomplished in the near term.

## IN THIS ISSUE

This special issue brings together articles from four teams that have devised architectures to meet these chal-

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lenges. All these architectures are grounded in established nanodevices and nanofabrication technologies. Two of the articles describe architectures that combine such nanodevices with microelectronics, using silicon-wafer technology as a platform for the ultradense integration of postsilicon features. A third article describes a seminal approach to designing computers that work without any microelectronics at all. The fourth article discusses and evaluates one of the hardest facts architects face when working with devices at the nanometer scale—namely, they must be exceptionally careful if they are to design a computer that is reliable at the system level.

In "From Synapses to Circuitry: Using Memristive Memory to Explore the Electronic Brain," Greg Snider and his colleagues at Hewlett-Packard Laboratories and Boston University present an architecture for an emulator of large-scale "brain like" networks and algorithms. Emulating networks at this scale requires using an ultra-tiny electronic equivalent of biological synapses, which are the key interconnection points in the brain's networks. To accomplish this, the authors propose using a "memory resistor" device termed the *memristor*. In 2008, R. Stanley Williams's team at Hewlett-Packard made headlines with its discovery that a large class of two-terminal nanodevices produces memristive current-voltage behavior. This article describes a plan to integrate these nanodevices into a processing-in-memory architecture that is the root of a hybrid micro/nano brain-like computing hierarchy.

In "Computing with Novel Floating-Gate Devices," Daniel Schinke and his North Carolina State University colleagues describe a "unified memory" nanodevice that is suitable for replacing the different kinds of memory found in both computers and field-programmable gate arrays. This nanocrystal device is faster than flash memory and can withstand many more write-erase cycles. Thus, the authors propose architectures in which the nanocrystal device replaces the DRAM in main memory or the SRAM in a programmable interconnect, making it much denser. Furthermore, since it is nonvolatile, manufacturers could use the device to enable true "instant-on" computers.

In "Crystals and Snowflakes: Building Computation from Nanowire Crossbars," André DeHon and Benjamin Gojman of the University of Pennsylvania show how computers might be implemented without silicon microelectronics at all, using instead a novel device called a *semiconducting nanowire*. The authors have developed a nanocomputer architecture that consists of organizing nanowire devices into structured lattices, much like crystals. In working out the details of this architecture, they recognize and deal with the fact that each crystal, fabricated using bottom-up chemical assembly methods, is likely to be unique—much like a snowflake.

"Toward Future Systems with Nanoscale Devices: Overcoming the Reliability Challenge," by Wenjing Rao of the University of Illinois at Chicago, Chengmo Yang of the University of Delaware, Ramesh Karri of the Polytechnic Institute of New York University, and Alex Orailoglu of the University of California, San Diego, confronts challenges implicit in the variations present in the devices and circuits that make up nanocomputers. The authors present a hierarchical approach to reliability that emphasizes redundancy, repair, and reconfiguration at the nanodevice level. At the system level, their approach employs topology-aware redistribution of code and data in the presence of faults. The techniques they recommend are likely to be effective not just for nanotechnologies beyond silicon, but also as it becomes prohibitively expensive to maintain ultrahigh yields during silicon-wafer manufacturing and processing.

These four articles provide an illuminating cross-section of the opportunities and challenges of computing in the nascent postsilicon era. They demonstrate ways in which we might transition from microelectronics to nanoelectronics, first by using hybrid architectures and, ultimately, by looking beyond conventional microtechnologies to novel postsilicon approaches. It is through such approaches that the nanocomputing community will continue to engineer seamless growth in the capability and complexity of computing systems for many years to come.

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